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COMPARATIVE STUDY OF NANOSCALE NMOS DEVICE'S STRUCTURE AND CHARACTERISTICS

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ABSTRACT

MOSFETs are employed in digital and analogue monolithic integrated circuits as discrete devices as well as active elements (ICs). The device feature size of such circuits has been reduced to the deep sub-micrometre range in recent years. In this research, a 180 nm NMOS and a 90 nm NMOS structure were built, simulated, and compared using Visual TCAD and GENIUS simulation software. Based on the simulation results, the best solution is found, with a threshold voltage of 0.4568V in the case of 180 nm NMOS and 0.2568V in the case of 0.2568V. The results are compared to the ITRS guidelines for devices with 180 nm and a 90 nm.

KEYWORDS: 180 nm NMOS, 90 nm NMOS Visual TCAD, Threshold voltage.

INTRODUCTION

Due to a major significant necessity for continuous circuit performance enhancement, the gate length of high-performance MOSFETs has been actively expanded year by year. The International Technology Roadmap for Semiconductors (ITRS) shows how the gate length of high-performance MOSFETs has been scaled in the past and how it will be scaled in the future [1]. This technology has advanced to the point where identical MOSFET production procedures are extensively employed in industry around the world [2]. Scaling Complementary Metal Oxide Semiconductor (CMOS) devices to smaller physical dimensions has been a driving force for the semiconductor industry to address market demand for increased integrated circuit functionality and performance at low cost. Smaller MOSFETs are desirable by main reasons:

1. Smaller MOSFETs allow more current to pass, because of the low resistance.

2. Smaller MOSFETs have smaller gates, and thus lower gate capacitance.

These two factors provide lower switching times, and thus higher speeds. Gate oxide thickness, channel doping, channel length, are varying factors that controlling threshold voltage (V_T) and caused device performance problems [5] [6]. V_T is important parameter which determines whether transistor works or not [5]. LDD and retrograde well are implemented to control short channel effect and hot carrier reliability [7]. Besides that, LDD is designed to smear out the strong electric field between the channel and heavily doped source or drain, to reduce hot carrier generation [5]. International Technology Roadmap for Semiconductor (ITRS) value in which V_T value should be 0.4625 ± 12.7% is being used as the target to achieve the objective of research.

DEVICE MATERIAL AND DESIGN

In MOSFET transistor the bottom rectangular block of material is the silicon substrate

often referred to as the bulk. There are four electronically active regions that are marked: *gate* (G), *source* (S), and *drain* (D), and the *bulk* terminal (B) to which the gate, drain, and source voltages are typically referenced.

Region	Material	Length/µm 180 nm	Length/µm 90 nm
Substrate	Silicon	0.29	0.29
Drain	Aluminium	0.10	0.10
Source	Aluminium	0.10	0.10
Gate	NpolySi	0.180	0.09
Oxide	Sio_2	0.35	0.25

Table 1 Regions and Material used in NMOS

A thin silicon oxide dielectric with thickness T_{OX} separates the rectangular gate region from the bulk. The transistor gate length and breadth are two more critical dimensions. The drain and source regions are implanted in the substrate; however, they are doped in the opposite direction. The electrical behaviour of semiconductor devices is calculated via device simulation. Table 1 shows regions and materials used in simulation of device. Table 2 shows doping, and profiles used in 180 nm device.

Name	Profile	Type	DOPING
Substrate	Uniform	Acceptor	3E17
Channel	Gaussian	Acceptor	1E18
LDD_S/LDD_D	Gaussian	Donor	4E19
Source/Drain	Gaussian	Donor	1E20

Table 2 Doping Profile of 180 nm

Table 3 shows doping, and profiles used in 90 nm device.

Name	Profile	Type	DOPING
Substrate	Uniform	Acceptor	3E17
Channel	Gaussian	Acceptor	1E13
LDD_S/LDD_D	Gaussian	Donor	5E19
Source/Drain	Gaussian	Donor	2E20

Table 3 Doping Profile of 90 nm

RESULT AND DISCUSSION

The simulation results of 180 nm and 90 nm NMOS can be viewed in the Tony Plot is shown below. GENIUS code has flexible mesh data structure which supports various shapes of 2D.

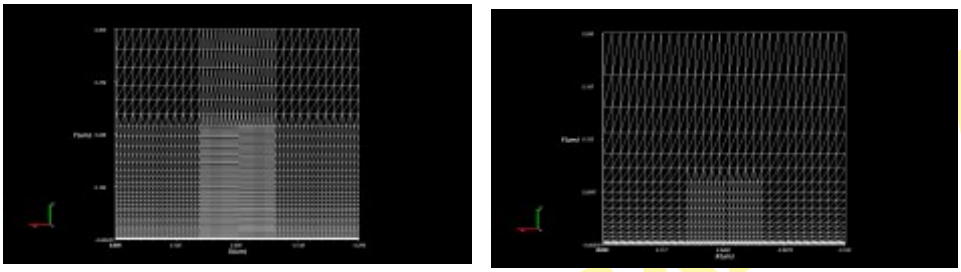

Figure 1: 180 nm and 90 nm device mesh respectively

The only limit is the element should have circum-circle for 2D or circum-sphere for 3D to meet finite volume method used by GENIUS. The supported element shapes can be triangle and quadrangle for 2D, tetrahedron, prism and hexahedron for 3D. In this research triangle is used. Figure 1 show the mesh layout of 180 nm and 90 nm device respectively on which final structure of this MOSFET device is implemented. It is base of device. Figure 2 shows holes and electrons concentration in devices.

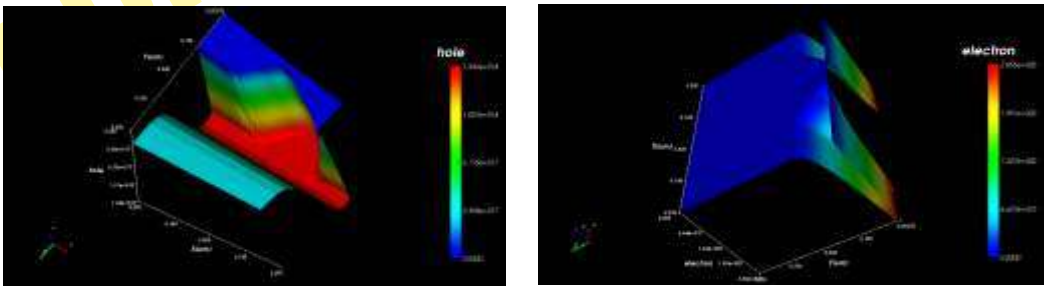

Figure 2: Holes and Electrons in devices

Holes are majority carrier and electrons are minority carrier in p type semiconductor. Holes are minority carrier and electrons are majority carrier in n type semiconductor. I_D –V_{GS} relationship of 180 nm and 90 nm compared in table 4.

S.No	V_{GS}(V)	I_D(A) 180nm	I_D(A) 90nm
1	0	1.81846e-11	9.86559e-10
2	0.2	4.41476e-09	3.82371e-07
3	0.4	1.36107e-06	2.89685e-05
4	0.6	3.13083e-05	0.000134861
5	0.8	0.000104931	0.000260298
6	0.9	0.000151492	0.000312779
7	1.1	0.000255525	0.000416174
8	1.3	0.000365978	0.000529069
9	1.4	0.00042109	0.000579853
10	1.5	0.000475273	0.00062131

Table 4 I_D –V_{GS} relationship at 180 nm and 90 nm channel length at V_{DS}=0.5V

Figure 3 shows that I_D versus V_{GS} comparison of 180 nm and 90 nm NMOS depending upon the value of table 4.

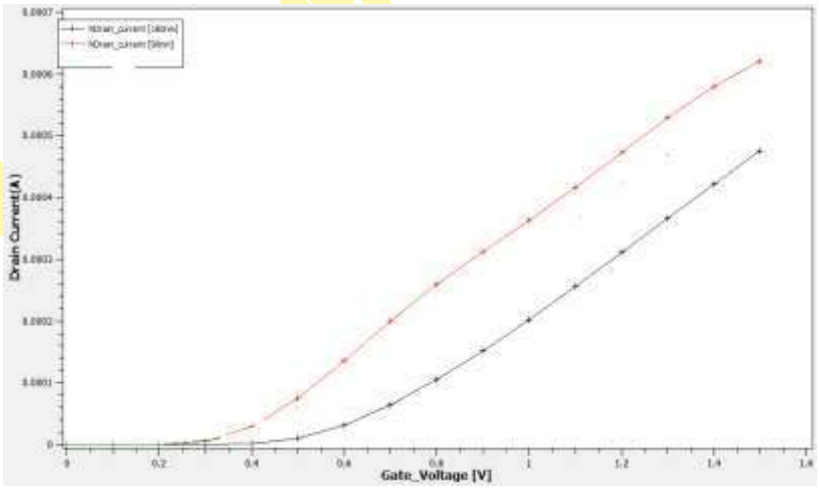

Figure 3 shows that I_D versus V_{GS} comparison of 180 nm and 90 nm NMOS

From figure 3 it is observed that threshold voltage of 90 nm NMOS is less than 180 nm NMOS.

S.No	V_{DS}(V)	I_D(A) 180nm	I_D(A) 90nm
1	0	1.04161e-16	1.58995e-16
2	0.2	0.000144231	0.000287246
3	0.4	0.00019595	0.000362006
4	0.6	0.000205621	0.000379311
5	0.8	0.000210609	0.000388089
6	1	0.000214603	0.000394936
7	1.2	0.000218096	0.000401039
8	1.4	0.000221274	0.000406753
9	1.6	0.000224178	0.000412345
10	1.8	0.00022688	0.000418251
11	2	0.000229459	0.000423801
12	2.2	0.000231945	0.00042887
13	2.4	0.000234338	0.000433748
14	2.5	0.000235498	0.000436159

Table 5. I_D –V_{DS} relationship at 180 nm and 90 nm channel length at V_{GS}=1V

I_D –V_{DS} relationship of 180 nm and 90 nm NMOS compared in table 5.Depending upon the value of table 5 the I_D versus V_{DS}characteristics are plots in figure 4.

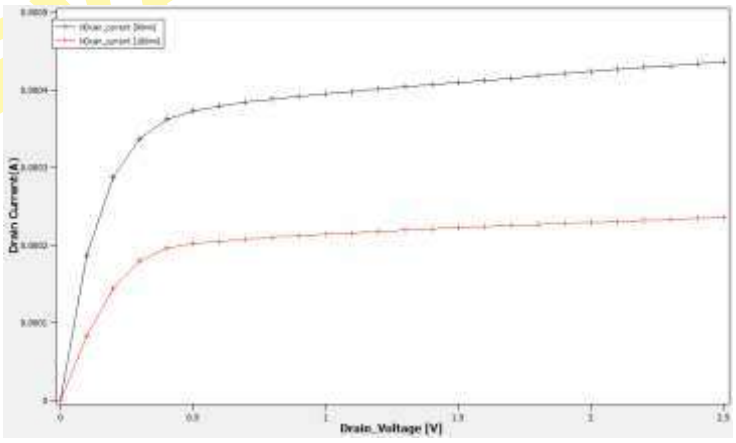

Figure 4 shows that I_D versus V_G comparison of 180 nm and 90 nm NMOS

It is observed from figure 4 I_D current is more in 90 nm NMOS as compared to 180 nm NMOS.

CONCLUSION

The Visual TCAD module is used to model the 180 nm and 90 nm NMOS MOSFETs. The electrical response of the NMOS can be simulated using the TCAD module. Characteristics are compared in this paper device construction. The ideal value of VT 0.4568V in the case of 180 nm and 0.2568V in the case of 90 nm is found from the simulation results. These values are in accordance with the ITRS NMOS device guideline.

REFERENCES

Optimization of Device Performance using TCAD Tools. Silvaco International product at:

www.silvaco.com/content/kbase/UMichigan_TCAD.pdf

R. Arghavani et. al. (2007). "High-k/Metal Gates Prepare for High-Volume Manufacturing". Semiconductor International. Reed Elsevier Inc.

Teoh Chin Hong, Razali Ismail. (2006). "Device Design Considerations for Nanoscale MOSFET Using Semiconductor TCAD Tools." IEEE: 906-910.

Taib Ziad Mohamad, Ibrahim ahamd, Azami Zaharim. (2008) "Optimum Solution in Fabricating 65nm NMOS Transistors Using Taguchi Method". ACACOSS: April: 6-8.

Xiangli Li, Stephen A. Parke, Bongdan M. Wilamowski. (2003). "Threshold Voltage Control for Deep Sub-micrometer Fully Depleted SOI MOSFET". IEEE: 284 – 287.

N. Sirisantana, L. Wei and K. Roy. (2000). "High-performance low-power CMOS circuits using multiple channel length and multiple oxide thickness". Proc. Int. Conf Computer Design, 227-232.

K. Schuegraf and C. Hu. (1994). "Hole injection breakdown model for very low voltage lifetime extrapolation". IEEE Transactions of Electron Device. Vol. 41: 761-767.

Maizan Muhamad, Sunaily Lokman, Hanim Hussian. (2009). "Optimization in fabrication 90 nm NMOS transistor using silvaco". Proceeding of 2009 IEEE student conference on Research and Development (SCOReD), 16- 18 Nov' 09, UPN Serdang, Malaysia.